

IN THE CLAIMS

1. (withdrawn) A method of making an electrode on a semiconductor structure, comprising:

a) depositing metal on a surface of a semiconductor structure;

b) forming a patterned mask over the metal on the semiconductor structure, the mask having at least one opening so that a first region is covered by the mask and a second region aligned with the at least one opening is left uncovered by the mask;

c) removing metal aligned with the at least one opening in the second region, so as to reveal the top surface of the semiconductor structure in the second region; and

d) removing material of the semiconductor structure aligned with the at least one opening in the second region.

2. (withdrawn) The method of claim 1, wherein the metal comprises a first metal and a second metal.

3. (withdrawn) The method of claim 2, wherein said first metal and second metal are selected to form a substantially transparent material upon annealing.

4. (withdrawn) The method of claim 3, further comprising annealing the first metal and second metal.

5. (withdrawn) The method of claim 4, wherein the first metal comprises nickel and the second metal comprises gold.

6. (withdrawn) The method of claim 2, wherein the step of depositing comprises electron beam deposition.

7. (withdrawn) The method of claim 6, wherein the step of depositing metal comprises depositing a first metal and depositing a second metal overlying the first metal.

8. (withdrawn) The method of claim 1, wherein the step of forming a patterned mask comprises applying a resist on the metal and lithographically patterning the resist to form the at least one opening over the second region so that the remaining resist overlies the semiconductor structure in the first region.

9. (withdrawn) The method of claim 8, wherein the step of removing metal comprises etching.

10. (withdrawn) The method of claim 9, wherein the step of etching comprises etching with KI:I2:DI solution.

11. (withdrawn) The method of claim 9, wherein the step of removing material from the semiconductor structure comprises etching the semiconductor structure while the resist remains over the semiconductor structure in the first region.

12. (withdrawn) The method of claim 10, wherein the step of removing material from the semiconductor structure comprises a reactive ion etching.

13. (withdrawn) The method of claim 12, wherein the step of etching comprises etching with BCl<sub>3</sub>.

14. (withdrawn) The method of claim 8, wherein the resist layer covering the first region has edges and the step of removing metal is performed so as to remove some of the metal underneath the resist layer adjacent the edges of the resist layer to form a space between the edges of the resist layer and the metal on the semiconductor structure.

15. (withdrawn) The method of claim 14, wherein the metal in the first region substantially covers the first region except in said space.

16. (withdrawn) The method of claim 1, wherein the step of removing material from the semiconductor structure in the second region is performed so as to leave the first region protruding from the remainder of semiconductor structure.

17. (withdrawn) The method of claim 16, wherein the semiconductor structure comprises a p-type semiconductor layer overlying an n-type semiconductor layer arranged beneath the p-type semiconductor layer, the semiconductor structure having a junction between the p-type layer and the n-type layer.

18. (withdrawn) The method of claim 17, wherein, after material is removed from the semiconductor structure in the second region, an upwardly protruding portion comprising the p-type layer and a lower region comprising a portion of the n-type layer are formed.

19. (withdrawn) The method of claim 17, wherein the metal covers a large portion of the semiconductor structure in the first region, the metal being in contact with the p-type layer.

20. (withdrawn) The method of claim 18, further comprising forming a lower electrode on the n-type layer of the second region.

21. (currently amended) A method of making a transparent electrode for a light-emitting diode, comprising:

a) depositing metal on a top surface of a semiconductor structure;

b) defining a first region of the semiconductor structure for a first electrode by forming a mask over the metal, the mask having at least one opening so that the first region is covered by the mask and a second region is aligned with the at least one opening in the mask;

c) removing metal aligned with the at least one opening in the mask in the second region to form the first

electrode overlying the first region of the semiconductor structure and so as to reveal the top surface of the semiconductor structure in the second region; and

d) after forming the first electrode during the removing metal step, removing material from the semiconductor structure aligned with the at least one opening in the second region to form a second electrode surface for a second electrode, the second electrode surface being lower in elevation than the top surface of the semiconductor structure.

22. (original) The method of claim 21, wherein the step of depositing metal includes depositing a first metal and depositing a second metal.

23. (original) The method of claim 22, further comprising annealing the first metal and second metal.

24. (original) The method of claim 22, wherein said first metal and second metal are selected to form a substantially transparent material upon annealing.

25. (original) The method of claim 22, wherein the first metal comprises nickel and the second metal comprises gold.

26. (original) The method of claim 21, wherein the step of depositing comprises electron beam deposition.

27. (original) The method of claim 23, wherein the step of depositing metal comprises depositing a first metal and depositing a second metal overlying the first metal.

28. (original) The method of claim 21, wherein the step of defining a first region comprises applying a resist on the metal, and lithographically patterning the resist to form at least one opening in the second region so that the remaining resist overlies the semiconductor structure in the first region.

29. (original) The method of claim 21, wherein the step of removing metal comprises etching.

30. (original) The method of claim 29, wherein the step of etching comprises etching with KI:I2:DI solution.

31. (original) The method of claim 29, wherein the step of removing material from the semiconductor structure comprises etching the semiconductor structure while the resist remains in the first region.

32. (original) The method of claim 31, wherein the step of removing material from the semiconductor structure comprises reactive ion etching.

33. (original) The method of claim 31, wherein the step of etching comprises etching with  $\text{BCl}_3$ .

34. (original) The method of claim 28, wherein the resist layer in the first region has edges and the step of removing metal is performed so as to remove some of the metal underneath the resist layer adjacent the edges of the resist layer to form a space between the edges of the resist layer and the metal on the semiconductor structure.

35. (original) The method of claim 34, wherein the metal in the first region substantially covers the first region except in said space.

36. (original) The method of claim 21, wherein the step of removing material from the semiconductor structure in the second region is performed so as to leave the first region protruding from the remainder of semiconductor structure.

37. (original) The method of claim 36, wherein the semiconductor structure comprises a p-type semiconductor layer

overlying an n-type semiconductor layer arranged beneath the p-type semiconductor layer, the semiconductor structure having a junction between the p-type layer and the n-type layer.

38. (original) The method of claim 37, wherein the first region comprises an upwardly protruding portion of the p-type layer and the second region comprises a portion of the n-type layer.

39. (original) The method of claim 38, wherein the first region forms the mesa of the light-emitting diode, and the metal forms an electrode on the mesa.

40. (original) The method of claim 37, wherein the metal covers a large portion of the semiconductor structure in the first region, the metal being in contact with the p-type layer.

41. (original) The method of claim 37, further comprising forming a lower electrode on the n-type layer of the second region.